DSP-L138

Baseboard

User's Manual

Edition 1.11
2015/09/24

Copyright

Copyright 2013, all rights reserved. This document is copyrighted and all rights are reserved. The information in this document is subject to change without prior notice to make improvements to the products.
This document contains proprietary information and protected by copyright. No part of this document may be reproduced, copied, or translated in any form or any means without prior written permission of the manufacturer.
All trademarks and/or registered trademarks contains in this document are property of their respective owners.

Disclaimer

The company shall not be liable for any incidental or consequential damages resulting from the performance or use of this product.
The company does not issue a warranty of any kind, express or implied, including without limitation implied warranties of merchantability or fitness for a particular purpose.
The company has the right to revise the manual or include changes in the specifications of the product described within it at any time without notice and without obligation to notify any person of such revision or changes.

Trademark

All trademarks are the property of their respective holders.

Any questions please visit our website at http://www.commell.com.tw

Packing List:

Please check the package content before you starting using the board.

1 x DSP-L138 Baseboard

2 x stereo audio cables

Options:

D13-080SUTB00A0-S V1.0
(800x600 LCD with touch screen)

SPD-030-5

OALLCD-T18C-C01:

(LCD Cable for D13-080SUTB00A0-S)

Index

Chapter 1 <Introduction> 0

1.1 <Product Overview> 0
1.2 <Product Specification> 3
1.3 <Photograph> 5
1.4 <Block Diagram> 0

Chapter 2 <Hardware setup> 1

2.1 <Connector & Jumper Location> 1
2.2 <Connectors and Jumpers Setting> 0
2.2.1 <Connectors and Jumpers> 0
2.2.2 <Switches> 0
2.5 <I/O interface> 1
2.5.1 <Serial ATA interface> 1
2.5.2 <Ethernet interface> 0
2.5.3 <Display interface> 0
2.5.4 <Audio interface> 1
2.5.5 <USB interface> 0
2.5.6 <COM1 interface> 0
2.5.7 <MMC/SD slot> 0
2.5.8 <J11> 0
2.5.9 <JTAG> 0
2.5.10 <CN_IO> 0
2.5.11 <CN_IO1> 0
2.5.12 <CN_IO2> 0
2.5.13 <USB-XDS100> 0

2.6 <Power supply>.....0

Appendix A <Boot SD Card>.....0

Appendix C <References>.....0

Contact information.....0

Chapter 1 <Introduction>

1.1 <Product Overview>

DSP-L138 is a motherboard that based on Texas Instruments OMAP-L138 C6-Integra DSP+ARM Processor to implement most useful features and functionalities of this integrated processor. This motherboard is designed to be a development board for customers to implement and verify their applications for OMAP-L138 features. TI DVSDK is the software support of this product.

The OMAP-L138 C6-Integra DSP+ARM processor is a low-power applications processor based on an ARM926EJ-S and a C674x DSP core. It provides significantly lower power than other members of the TMS320C6000 platform of DSPs.

The device enables OEMs and ODMs to quickly bring to market devices featuring robust operating systems support, rich user interfaces, and high processing performance life through the maximum flexibility of a fully integrated mixed processor solution.
The dual-core architecture of the device provides benefits of both DSP and Reduced Instruction Set Compute (RISC) technologies, incorporating a high-performance TMS320C674x DSP core and an ARM926EJ-S core.

The ARM926EJ-S is a 32-bit RISC processor core that performs 32-bit or 16-bit instructions and processes 32-bit, 16-bit, or 8-bit data. The core uses pipelining so that that all parts of the processor and memory system can operate continuously.

The ARM core has a coprocessor 15 (CP15), protection module, and Data and program Memory Management Units (MMUs) with table look-aside buffers. It has separate 16K-byte instruction and 16K-byte data caches. Both are four-way associative with virtual index virtual tag (VIVT). the ARM core also has a 8KB RAM (Vector Table) and 64KB ROM.

The device DSP core uses a two-level cache-based architecture. The level 1 program

cache (L1P) is a 32KB direct mapped cache and the Level 1 data cache (L1D) is a 32KB 2-way set-associative cache. The Level 2 program cache (L2P) consists of a 256KB memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or combinations of the two. Although the DSP L2 is accessible by ARM and other hosts in the system, an additional 128KB RAM shared memory is available for use by other hosts without affecting DSP performance.

ARM926EJ-S Core

- 32-Bit and 16-Bit (Thumb) Instructions
- DSP Instruction Extensions
- Single Cycle MAC
- ARM Jazelle Technology
- EmbeddedICE-RT for Real-Time Debug

ARM9 Memory Architecture

- 16K-Byte Instruction Cache
- 16K-Byte Data Cache
- 8K-Byte RAM (Vector Table)
- 64K-Byte ROM

C674x Instruction Set Features

- Superset of the C67x+ and C64x+ ISAs
- Up to 3648/2746 C674x MIPS/MFLOPS
- Byte-Addressable (8-/16-/32-/64-Bit Data)
- 8-Bit Overflow Protection
- Bit-Field Extract, Set, Clear
- Normalization, Saturation, Bit-Counting
- Compact 16-Bit Instructions

C674x Two Level Cache Memory Architecture

- 32K-Byte L1P Program RAM/Cache
- 32K-Byte L1D Data RAM/Cache

- 256K-Byte L2 Unified Mapped RAM/Cache
- Flexible RAM/Cache Partition (L1 and L2)

Enhanced Direct-Memory-Access Controller 3 (EDMA3):

- 2 Channel Controllers
- 3 Transfer Controllers
- 64 Independent DMA Channels
- 16 Quick DMA Channels
- Programmable Transfer Burst Size

TMS320C674x Floating-Point VLIW DSP Core

- Load-Store Architecture With Non-Aligned Support
- 64 General-Purpose Registers (32 Bit)
- Six ALU (32-/40-Bit) Functional Units
- Two Multiply Functional Units
- Instruction Packing Reduces Code Size
- All Instructions Conditional

Software Support

- TI DSP/BIOS
- Chip Support Library and DSP Library

Memory

- DDR2/Mobile DDR Memory Controller
- 128K-Byte RAM Shared Memory
- 1.8V or 3.3V LVCMOS IOs

Programmable Real-Time Unit Subsystem (PRUSS)

- Two Independent Programmable Realtime Unit (PRU) Cores
- Standard power management mechanism
- Dedicated interrupt controller
- Dedicated switched central resource

One Multichannel Audio Serial Port

- Two Clock Zones and 16 Serial Data Pins
- Supports TDM, I2S, and Similar Formats

- DI-Capable
- FIFO buffers for Transmit and Receive

Two Multichannel Buffered Serial Ports

- Supports TDM, I2S, and Similar Formats
- AC97 Audio Codec Interface
- Telecom Interfaces (ST-Bus, H100)
- 128-channel TDM
- FIFO buffers for Transmit and Receive

Serial ATA (SATA) Controller

- Supports SATA I (1.5 Gbps) and SATA II (3.0 Gbps)
- Supports all SATA Power Management Features
- Hardware-Assisted Native Command Queuing (NCQ) for up to 32 Entries
- Supports Port Multiplier and Command-Based Switching

Others

- Real-Time Clock With 32 KHz Oscillator and Separate Power Rail
- Three 64-Bit General-Purpose Timers (Each Configurable as Two 32-Bit Timers)
- One 64-Bit General-Purpose/Watchdog Timer (Configurable as Two 32-bit General-Purpose Timers)

1.2 <Product Specification>

System

Processor	TI OMAP-L138 Dual-Core SoC 1x ARM926EJ-S RISC MPU 1x C674x Fixed and Floating-Point VLIW DSP
Speed	ARM926 @ 456 MHz C674x DSP @ 456 MHz
Memory	128 MB DDR2 SDRAM
Boot Mode	Configurable boot mode
Real Time Clock	Integrated RTC with onboard lithium battery
Debug	XDS100 emulation circuit

Display

LCD Control	Maximum resolution is 1024 x 1024 pixels
Display	Default to 800 x 600 TFT LCD display panel
Touch	4-wire resistive 800 x 600 touch screen

Software Support

TI DVSDK	Linux 2.6.37 for ARM TI DSP/BIOS TI Chip Support Library TI DSP Library

I/O

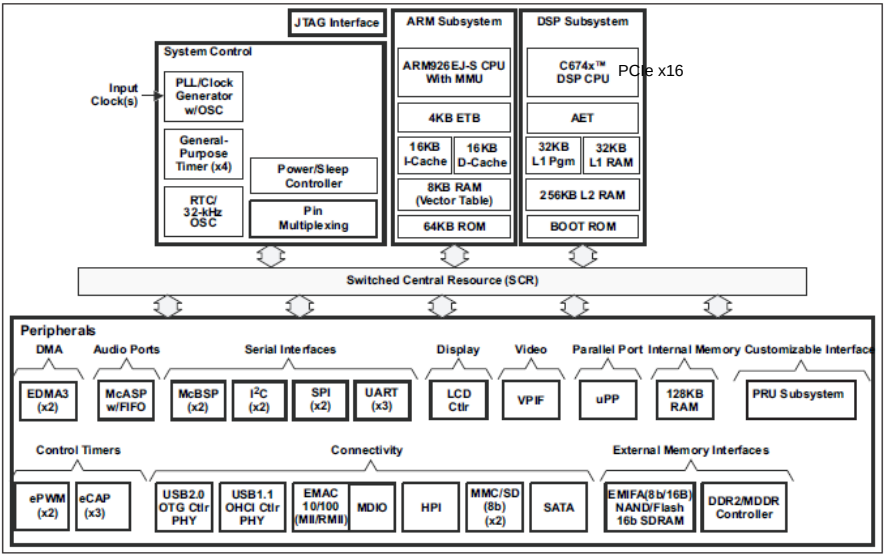
Flash Support	1x 8GB SPI flash chip (onboard) 1x MMC/SD card slot
Serial ATA	Support both SATA I and SATA II
Audio	TI TLV320AIC3106 Stereo Audio CODEC
LAN	EMAC provides 10Base-T and 100Base-TX
Internal I/O	1 x SATA2, 1 x TFT/STN, 1 x Line in , 1 x Line out
External I/O	1 x RS232, 1 x USB2.0 OTG, 1 x USB1.1 OHCI, 1 x MMC/SD,1 x RJ45 , 1 x DC connector .
Debug	XDS100 emulation (via USB interface)

Mechanical & Environmental

Power Requirement	DC Input 5V
Size & Thickness	170.8mm x 116.8mm (L x W)
Temperature	Operating within 0°C~60°C (32°F~140°F) Storage within -20°C~80°C (-4°F~176°F)
Relative Humidity	10%~90%, non-condensing

1.3 <Photograph>

1.4 <Block Diagram>

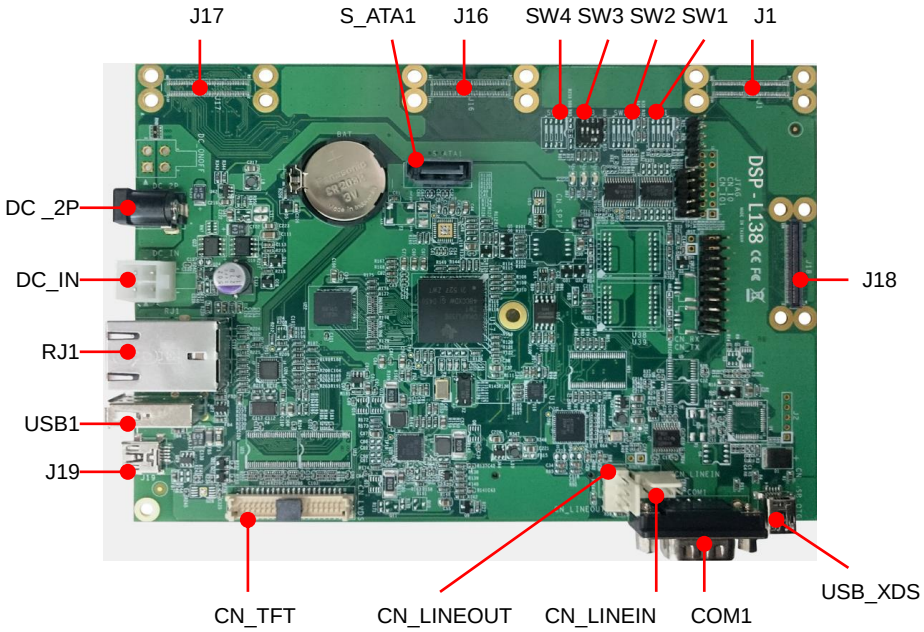


(1) Note: Not all peripherals are available at the same time due to multiplexing.

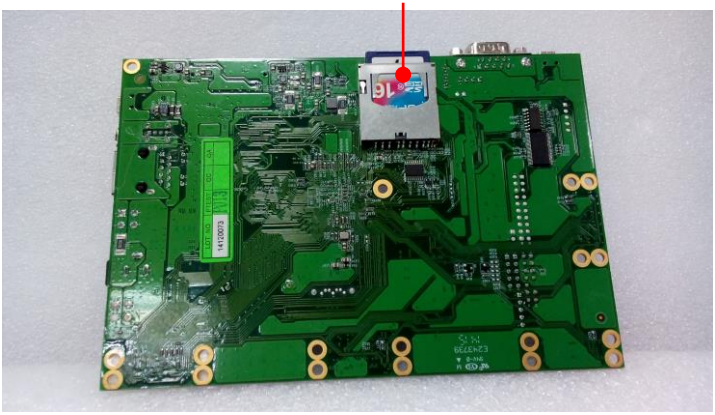
Figure 1-1. Functional Block Diagram

Chapter 2 <Hardware setup>

2.1 <Connector & Jumper Location>



SD Card Slot



2.2 <Connectors and Jumpers Setting>

2.2.1 <Connectors and Jumpers>

Location	Function
DC_2P	DC 5V input
DC_IN	Alternative DC 5V input
RJ1	10 Base-T / 100 Base-TX Mbps Ethernet
USB1	USB host
J19	USB OTG
CN_TFT+	Connect to TFT display panel and touch screen
CN_LINEOUT	Stereo audio output
CN_LINEIN	Stereo audio input
COM1	COM1 (Linux console if boot up with companion SD card)
USB_XDS	XDS100 debug via USB port interface
J18	Expansion J18
J1	Expansion J1
SW1	DIP switch 1
SW2	DIP switch 2
SW3	DIP switch 3
SW4	DIP switch 4
J16	Expansion J16
S_ATA1	SATA interface
J17	Expansion J17
MMC/SD slot	Slot for MMC/SD card (back side)

2.2.2 <Switches>

SW3: Boot mode setting

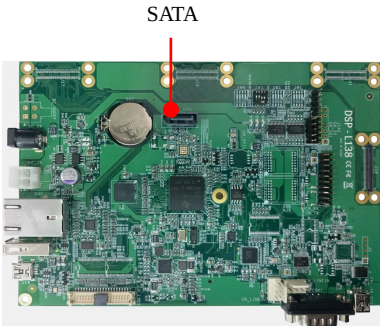
Jumper settings	Function
SW3:1	BOOT[4]
SW3:2	BOOT[3]
SW3:3	BOOT[2]
SW3:4	BOOT[1]

Boot Mode	BOOT4	BOOT3	BOOT2	BOOT1
NOR EMIFA	OFF	ON	ON	ON
NAND-8 EMIFA	OFF	OFF	OFF	ON
SPI1 Flash	OFF	OFF	OFF	OFF
UART2	ON	ON	OFF	OFF

EMU Debug	ON	OFF	OFF	ON

2.5 <I/O interface>

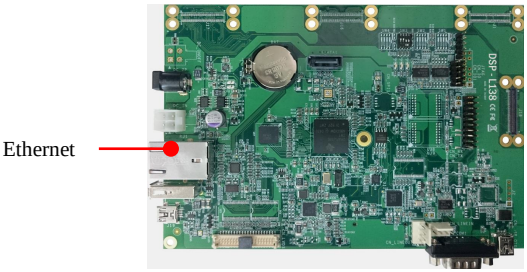
2.5.1 <Serial ATA interface>



SATA2: SATA 7-pin connector

Pin	Signal
1	GND
2	A+ (Transmit)
3	A- (Transmit)
4	GND
5	B- (Receive)
6	B+ (Receive)
7	GND

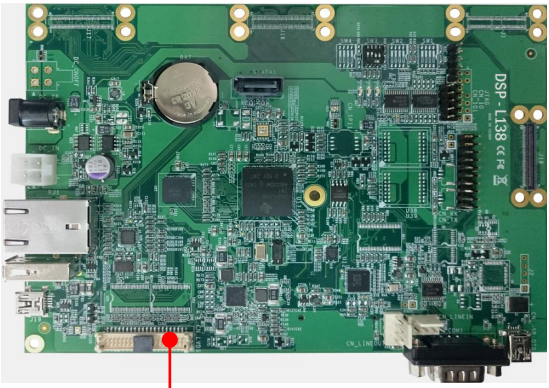
2.5.2 <Ethernet interface>



Ethernet: RJ45 10BASE-T / 100BASE-TX connector

Pin	Signal
1	TX+
2	TX-
3	RX+
4	N/A
5	N/A
6	RX-
7	N/A
8	N/A

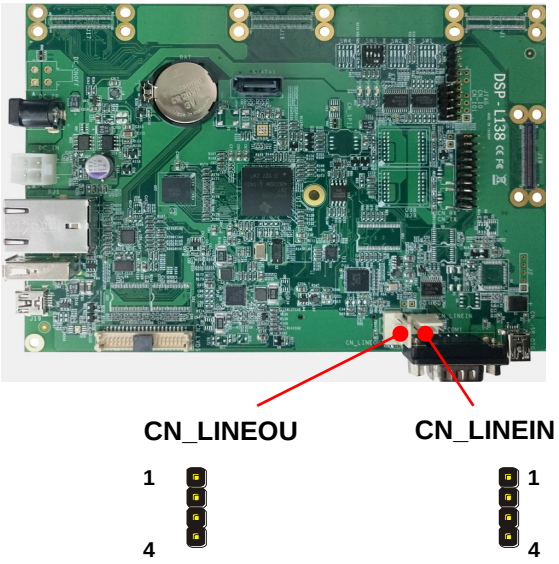
2.5.3 <Display interface>



CN_TFT+:

Pin	Signal	Pin	Signal
1	LCD_BACKLIGHT_PWR	**2**	LCD_PANEL_POWER
3	GND	**4**	GND
5	+5V	**6**	+3.3V
7	+5V	**8**	+3.3V
9	GND	**10**	GND
11	LCD_R1	**12**	LCD_R2
13	LCD_R3	**14**	LCD_R4
15	LCD_R5	**16**	LCD_G0
17	LCD_G1	**18**	LCD_G2
19	LCD_G3	**20**	LCD_G4
21	LCD_G5	**22**	LCD_B1
23	LCD_B2	**24**	LCD_B3
25	LCD_B4	**26**	LCD_B5
27	N/C	**28**	LCD_MDISP
29	LCD_DCLK	**30**	LCD_VSYNC
31	LCD_PWM0	**32**	LCD_HSYNC
33	N/C	**34**	N/C
35	TOUCH_LEFT	**36**	TOUCH_TOP
37	TOUCH_RIGHT	**38**	TOUCH_BOTTOM
39	GND	**40**	GND

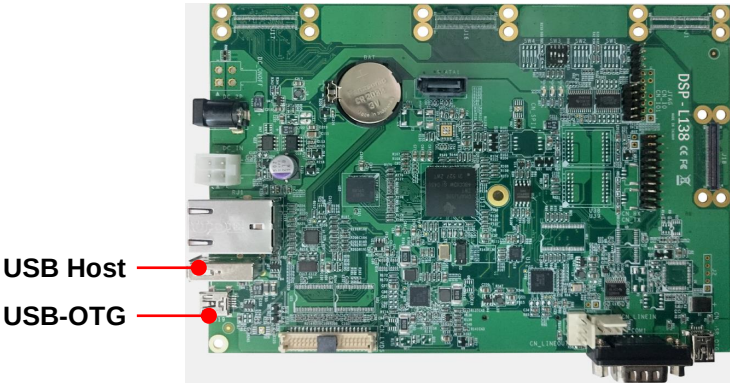
2.5.4 <Audio interface>



CN_LINEIN / CN_LINEOUT:

Pin	Signal
1	LEFT+
2	LEFT- / GND
3	RIGHT- / GND
4	RIGHT+

2.5.5 <USB interface>



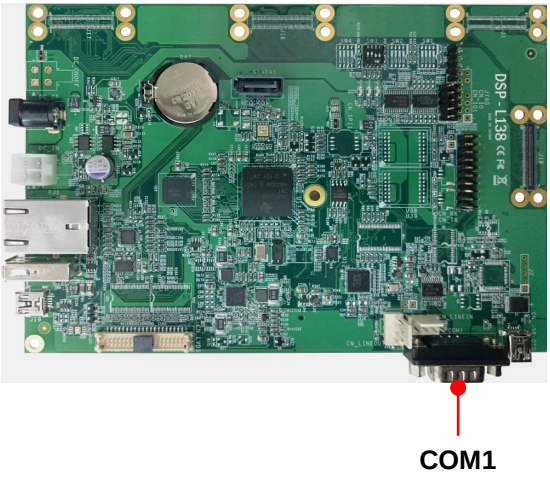
USB1:

Pin	Signal	Pin	Signal
1	USB1_VBUS (5V)	**2**	USB1_D-
3	USB1_D+	**4**	DGND
5	GND	**6**	GND

USB0-OTG:

Pin	Signal	Pin	Signal
1	USB0_VBUS (5V)	**2**	USB0_D-
3	USB0_D+	**4**	USB0_ID
5	DGND		

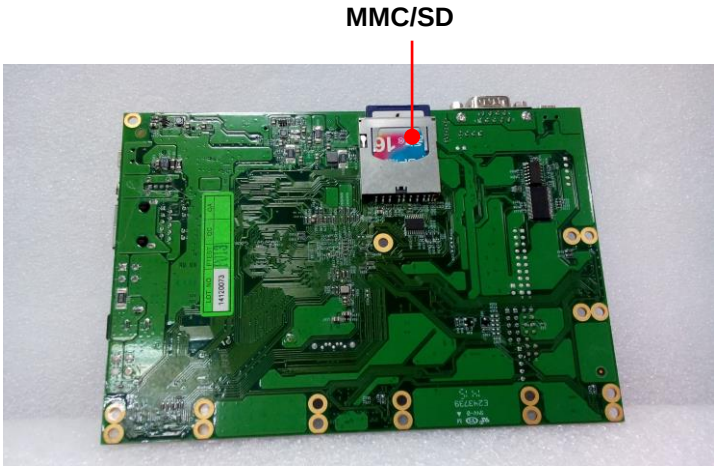
2.5.6 <COM1 interface>



COM1: RS232 DB9 connector

Pin	Signal	Pin	Signal
1	N/C	**2**	RXD
3	TXD	**4**	N/C
5	GND	**6**	N/C
7	RTS	**8**	CTS
9	N/C		

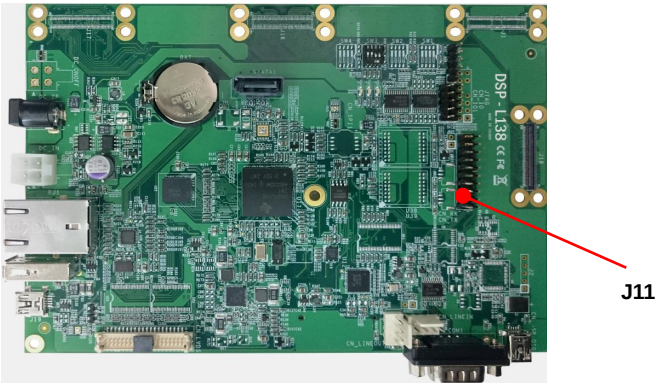
2.5.7 <MMC/SD slot>



MMC/SD:

Pin	Signal	Pin	Signal
1	DATA3	**2**	CMD
3	VSS1	**4**	VDD
5	CLK	**6**	VSS2
7	DATA0	**8**	DATA1
9	DATA2	**10**	WP
11	CD#	**12**	GND
13	GND		

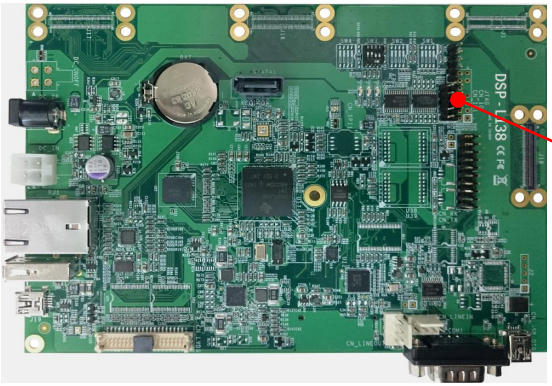
2.5.8 <J11>



J11: ARM JTAG (Multi-ICE)

Pin	Signal	Pin	Signal
2	IO_3.3V_1.8V	**1**	IO_3.3V_1.8V
4	GND	**3**	JTAG_TRSTn
6	GND	**5**	JTAG_TDI
8	EMU_STS	**7**	JTAG_TMS
10	GND	**9**	JTAG_TCK
12	GND	**11**	JTAG_RTCK
14	GND	**13**	JTAG_TDO
16	GND	**15**	MSTR_nRST
18	GND	**17**	N/C
20	GND	**19**	N/C

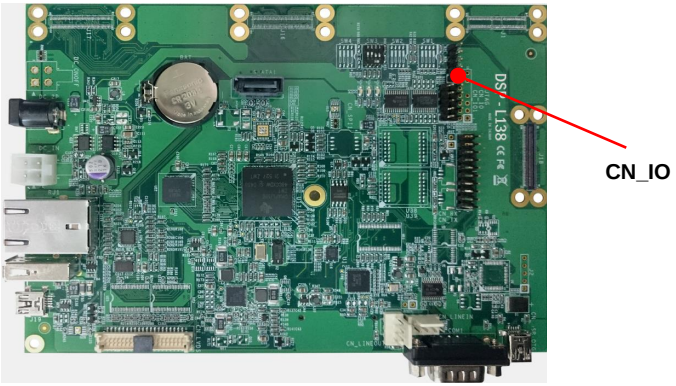
2.5.9 <JTAG>



JTAG: TI Rev B JTAG Interface

Pin	Signal	Pin	Signal
1	JTAG_TRSTn	**2**	JTAG_TMS
3	GND	**4**	JTAG_TDI
5	GND	**6**	IO_3.3V_1.8V
7	EMU_STS	**8**	JTAG_TDO
9	N/C	**10**	JTAG_RTCK
11	GND	**12**	JTAG_TCK
13	JTAG_EMU1	**14**	JTAG_EMU0

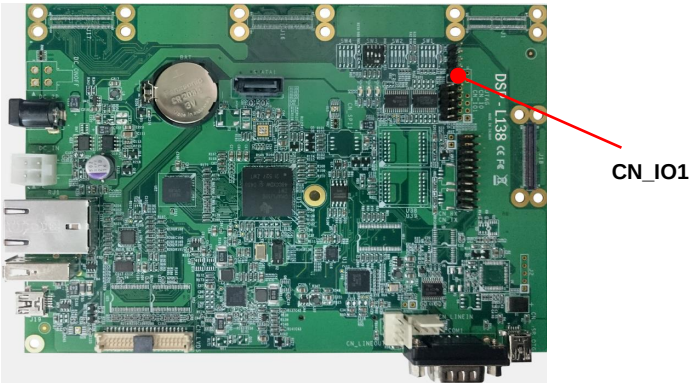
2.5.10 <CN_IO>



CN_IO:

Pin	Signal	Pin	Signal
1	IO0_3	**2**	IO0_4
3	IO0_5	**4**	IO0_6
5	IO0_7		

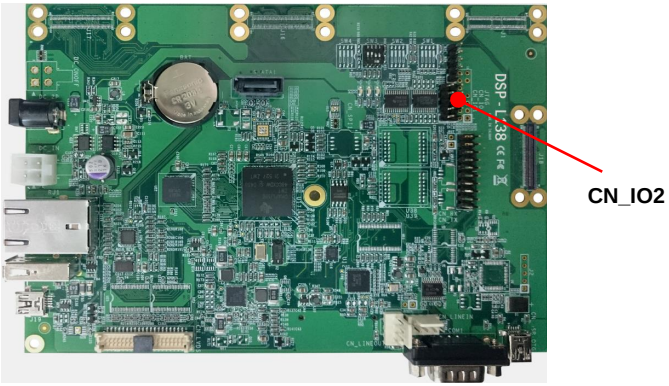
2.5.11 <CN_IO1>



CN_IO1:

Pin	Signal	Pin	Signal
1	IO0_6	**2**	IO0_7
3	IO1_0	**4**	IO1_1
5	IO1_2		

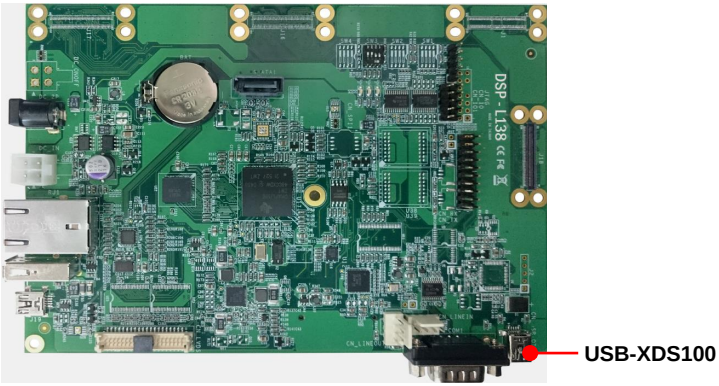
2.5.12 <CN_IO2>



CN_IO2:

Pin	Signal	Pin	Signal
1	IO1_3	**2**	IO1_4
3	IO1_5	**4**	IO1_6
5	IO1_7		

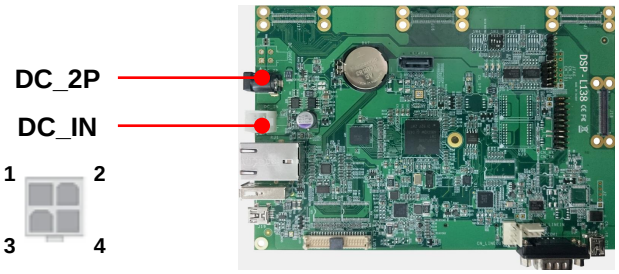
2.5.13 <USB-XDS100>



USB-XDS100: XDS100 USB Emulator

Pin	Signal	Pin	Signal
1	5V_USB	**2**	USBDM
3	USB_DP	**4**	N/C
5	GND		

2.6 <Power supply>



DC_IN: ATX12V 4-pin connector

Pin	Signal	Pin	Signal
1	GND	**2**	GND
3	5V	**4**	5V

DC_2P:

Pin	Signal	Pin	Signal
1	GND	**2**	GND
3	5V		

Appendix A <Boot SD Card>

A bootable SD card is shipped with the DSP-L138 board. This SD card boots TI Arago Linux 2.6.

This Linux DVSDK SD card comes with the START HERE folder. Please refer the setup.htm for more information.

For community support, please visit:
www.ti.com/e2e

The TI Embedded Processor Wiki is:

processors.wiki.ti.com

Appendix C <References>

1	SPRS586D: TI OMAP-L138 Datasheet
2	OMAPL138 Software Developers Guide
3	dvsdk_4_03_00_06_omapl138_Release_Notes
4	OMAP-L138 Software Design Guide
5	SPRUH77A: OMAP-L138 DSP+ARM Processor Technical Reference Manual
6	SPRAB62: TMS320C674x/OMAP-L1x Introductory Information

Contact information

Any advice or comment about our products and service, or anything we can help you please don't hesitate to contact with us. We will do our best to support you for your products, projects and business.

Taiwan Commate computer Inc.

Address	19F., NO.94, Sec. 1, Xintai 5th Rd., Xizhi Dist., New Taipei City 22102, Taiwan.
TEL	+886-2-26963909
FAX	+886-2-26963911
Website	www.commell.com.tw
E-mail	info@commell.com.tw (General infomation) tech@commell.com.tw (Technical Support)

Commell is a brand name of Taiwan Commate computer Inc.